AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1. (previously presented) A signal processing semiconductor integrated circuit device, comprising:

a reception-system circuit including,

a first amplifier circuit which amplifies a received signal;

a frequency converter which combines the amplified signal with an oscillation signal having a predetermined frequency to thereby effect frequency conversion on the combined signal; and

a second amplifier circuit which is DC-coupled to the frequency converter and amplifies the signal frequency-converted by the frequency converter;

said signal processing semiconductor integrated circuit device having a first operation mode in which the reception-system circuit is activated and a second operation mode in which the reception-system circuit is deactivated;

wherein voltage reference circuits, which respectively generate bias voltages for current sources for supplying operating currents for the frequency converter and the second amplifier circuit, are activated in response to a transition

from the second operation mode to the first operation mode, and thereafter the bias voltages are transferred to the current sources of the frequency converter and the second amplifier circuit to thereby activate the frequency converter and the second amplifier circuit.

2. (previously presented) The signal processing semiconductor integrated circuit device according to claim 1, wherein after the bias voltages are transferred to the current sources of the frequency converter and the second amplifier circuit, the second amplifier circuit performs a calibration for reducing a DC offset included in an output signal, and the first amplifier circuit is activated after the elapse of a predetermined time.

3. (original) The signal processing semiconductor integrated circuit device according to claim 2, wherein the second amplifier circuit comprises a plurality of amplifying stages, and each of the amplifying stages performs a calibration for reducing a DC offset included in an output signal.

4. (previously presented) The signal processing semiconductor integrated circuit device according to claim 3, wherein the voltage reference circuits are provided in plural

form in association with each of the first amplifier circuit, the frequency converter and the second amplifying circuit.

5. (previously presented) The signal processing semiconductor integrated circuit device according to claim 1, wherein a third amplifier circuit is connected to the input side of the frequency converter, and after the voltage reference circuits are activated, bias voltages produced therefrom are transferred to their corresponding current sources of the third amplifier circuit, the frequency converter and the second amplifier circuit, so that the second amplifier circuit performs a calibration for reducing a DC offset included in an output.

6. (original) The signal processing semiconductor integrated circuit device according to claim 5, wherein after the completion of the calibration by the second amplifier circuit, the transfer of the bias voltage to the current source of the third amplifier circuit is interrupted, and the transfer of the bias voltage to the current source of the first amplifier circuit is carried out.

7. (previously presented) The signal processing semiconductor integrated circuit device according to claim 1, further comprising:

a transmission-system circuit which modulates a transmit signal and combines the modulated signal with an oscillation signal to thereby effect frequency conversion on the combined signal;

a control-system circuit which controls the reception-system circuit and the transmission-system circuit; and

an oscillation-system circuit which generates an oscillation signal or an oscillation control signal combined by the reception-system circuit and the transmission-system circuit,

all being formed on a single semiconductor substrate.

8. (previously presented) A wireless communication system, comprising:

a signal processing semiconductor integrated circuit device according to claim 7; and

a baseband circuit which performs signal processing for performing the conversion of a signal outputted from the reception-system circuit to a voice signal and the conversion of the voice signal to the transmit signal, and controls the signal processing semiconductor integrated circuit device;

wherein a first command signal for activating the voltage reference circuits and a second command signal for activating the frequency converter and the second amplifier circuit are supplied from the baseband circuit.

9. (previously presented) The wireless communication system according to claim 8, wherein the first command signal for activating the voltage reference circuits and the second command signal for activating the frequency converter and the second amplifier circuit are supplied from the baseband circuit to the control-system circuit.

10. (previously presented) A method of controlling a signal processing semiconductor integrated circuit device which comprises a reception-system circuit including a first amplifier circuit which amplifies a received signal; a frequency converter which combines the amplified signal with an oscillation signal having a predetermined frequency to thereby effect frequency conversion on the combined signal; and a second amplifier circuit which is DC-coupled to the frequency converter and amplifies the signal frequency-converted by the frequency converter, the signal processing semiconductor integrated circuit device having a first operation mode in which the reception-system circuit is activated and a second operation mode in which the reception-

system circuit is deactivated, said method comprising the steps of:

activating voltage reference circuits, which respectively generate bias voltages for current sources for supplying operating currents for the frequency converter and the second amplifier circuit, in response to a transition from the second operation mode to the first operation mode; and

after the elapse of a predetermined time, transferring the bias voltages to the current sources of the frequency converter and the second amplifier circuit to thereby activate the frequency converter and the second amplifier circuit respectively.

11. (previously presented) The signal processing semiconductor integrated circuit device according to claim 7, wherein a third amplifier circuit is connected to the input side of the frequency converter, and wherein after the voltage reference circuits are activated, bias voltages produced therefrom are transferred to their corresponding current sources of the third amplifier circuit, the frequency converter and the second amplifier circuit, so that the second amplifier circuit performs a calibration for reducing a DC offset included in an output.

12. (previously presented) The signal processing semiconductor integrated circuit device according to claim 11, wherein after the completion of the calibration by the second amplifier circuit, the transfer of the bias voltage to the current source of the third amplifier circuit is interrupted, and the transfer of the bias voltage to the current source of the first amplifier circuit is carried out.

13. (new) The signal processing semiconductor integrated circuit device according to claim 1, wherein after the voltage reference circuits are activated, bias voltages produced therefrom are transferred to corresponding current sources of a third amplifier circuit, the frequency converter and the second amplifier circuit, so that the second amplifier circuit performs a calibration for reducing a DC offset included in an output.

14. (new) The signal processing semiconductor integrated circuit device according to claim 13, wherein after the completion of the calibration by the second amplifier circuit, the transfer of the bias voltage to the current source of the third amplifier circuit is interrupted, and the transfer of the bias voltage to the current source of the first amplifier circuit is carried out.